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Name: CHRISTINE HIGGINS

Signature

1/31/2000
Signature Date

Docket No. : SUMT-P001

APPLICATION TRANSMITTAL LETTER

Assistant Commissioner of Patents
United States Patent and Trademark Office
Washington, D.C. 20231
ATTN: BOX PATENT APPLICATION

Sir:

Transmitted herewith for filing is the patent application of
Inventor(s): **MYERS, T. *et al.***
Entitled: **SELECTABLE ANALOG FUNCTIONS ON A CONFIGURABLE DEVICE AND METHOD EMPLOYING NONVOLATILE MEMORY**

27 No. pages of specification, including title page, claims and abstract
6 No. sheets of X informal, ____formal drawings

Also enclosed are:
X Executed Combined Declaration and Power of Attorney for Patent Application
X An Original Executed Assignment of the Application
X Form PTO-1595 (Recordation Cover Sheet for Assignment)
X Verified Statement Claiming Small Entity Status with Cover Sheet
___ An Information Disclosure Statement (Form PTO-1449A and Form PTO-1449B)
___ A copy of References cited in Information Disclosure: _____ documents

FEES DUE
The fees due for filing the application pursuant to 37 C.F.R. 1.16 and for recording the Assignment, if any, are determined as follow:

CLAIMS					
	No. of Claims		Extra Claims	Rate	Fees
Basic Application Fee ($690 large entity; $345 small entity)					$ 345.00
Total Claims	20	Minus 20 =	0	X $18 = X $ 9 (small) =	.00
Total Independent Claims	3	Minus 3 =	0	X $78 = X $39 (small) =	.00
If Multiple Dependent Claims are presented, add $260.00 or $130.00(small)					
If Assignment enclosed, add Assignment Recording Fee $40.00					40.00
TOTAL APPLICATION FEE DUE					$ 385.00

PAYMENT OF FEES
The full fee due in connection with this communication is and is provided as follows: $ 385.00

____ The Commissioner is hereby authorized to charge the fees associated with this communication or credit any overpayment to **Deposit Account No: 500482**. A duplicate copy of this authorization is enclosed.

__X__ A Check No. 4235 for the above specified full fee is enclosed. However, in case Applicant inadvertently miscalculated any required fee, the Commissioner is hereby authorized to charge the necessary additional amount associated with this communication or credit any overpayment to **Deposit Account No: 500482**. A duplicate copy of this authorization is enclosed.

This application is filed pursuant to 37 C.F.R. 1.53 in the name of the above-identified Inventor(s).

Please direct all correspondence concerning the above-identified application to the following address:

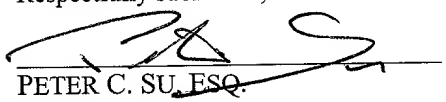
FERNANDEZ & ASSOCIATES, LLP
PATENT ATTORNEYS
PO BOX D
MENLO PARK, CA 94026-6204

(650) 325-4999
(650) 325-1203 : FAX
EMAIL: *iploft@iploft.com*

22877

PATENT TRADEMARK OFFICE

Respectfully submitted,



PETER C. SU, ESQ.
Reg. No. 43,939

1/31/2000
Date

02-02-00 A

The Assistant Commissioner of Patents
United States Patent and Trademark Office
Washington, D.C. 20231
ATTN: Box Patent Application

Re: U.S. Utility Patent Application
Appl. No. (Not yet assigned); Filed 1/31/2000
For: **SELECTABLE ANALOG FUNCTIONS ON A CONFIGURABLE DEVICE AND METHOD EMPLOYING NONVOLATILE MEMORY**
Inventor(s): **MYERS, T. *et al***
Docket No.: **SUMT-P001**

Sir:
The following documents are forwarded herewith for action by the U.S. Patent and Trademark Office:

1. U.S. UTILITY APPLICATION
entitled: **SELECTABLE ANALOG FUNCTIONS ON A CONFIGURABLE DEVICE AND METHOD EMPLOYING NONVOLATILE MEMORY**
having named inventor(s):
MYERS, T. *et al*
   a. a specification consisting:
      (i) 22 pages prior to the claims, including title page;
      (ii) 4 pages of claims;
      (iii) 1 page abstract;
   b. 6 sheets of **informal** drawings: (FIGs. 1-5);
2. An **original, executed** Combined Declaration and Power of Attorney by named inventors;
3. Form PTO-1082 (in duplicate);
4. Cover letter for Assignment (Form PTO-1595)
5. An original, executed Assignment to **SUMMIT MICROELECTRONICS, INC.**, executed by named inventors, recordation of which is hereby requested;
6. A return post card; and
7. Check No. 4235 for $ 385.00 to cover:

Patent application filing fee:	$ 345.00
Assignment Recordation fee:	$ 40.00
Excess claims fee:	$ .00

8. Verified Small Entity Status Statement with Cover Sheet

It is respectfully requested that the attached postcard be stamped with the filing date of the above documents and unofficial application number and returned to the addressee as soon as possible.

1/31/2000
Date

Respectfully submitted,

PETER C. SU, ESQ.
Reg. No. 43,939

FERNANDEZ & ASSOCIATES, LLP
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Docket No.: **SUMT-P001**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of :
Application No.: (Not yet assigned) Group No.: (Not yet assigned)
Filed: 1/31/2000 Examiner: (Not yet assigned)

Title: **SELECTABLE ANALOG FUNCTIONS ON A CONFIGURABLE DEVICE AND METHOD EMPLOYING NONVOLATILE MEMORY**

Inventor(s): **MYERS, T. *et al***

Assistant Commissioner for Patents
Washington, D.C. 20231

SUBMISSION OF VERIFIED STATEMENT TO ESTABLISH SMALL ENTITY STATUS

The attached statement is being submitted to establish small entity status in this

_X_ Application
___ Patent

by the

___ Independent inventor(s) 37 CFR 1.9(c) and 1.27(b)
___ Non-inventor supporting claim by another 37 CFR 1.9(c) and 1.27(b)
_X_ Small Business Concern 37 CFR 1.9(d) and 1.27(c)
___ Nonprofit Organization 37 CFR 1.9(e) and 1.27(d)

Respectfully submitted,

PETER C. SU, ESQ.
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Docket No.: **SUMT-P001**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: (Not yet assigned)
Filed on: 1/31/2000

Patent No.: (Not yet assigned)
Issued on: (Not yet assigned)

Title: **SELECTABLE ANALOG FUNCTIONS ON A CONFIGURABLE DEVICE AND METHOD EMPLOYING NONVOLATILE MEMORY**

Inventor(s): **MYERS, T. *et al***

VERIFIED STATEMENT CLAIMING SMALL ENTITY STATUS

(37 CFR 1.9(f) and 1.27(c) -- SMALL BUSINESS CONCERN)

I hereby declare that I am

____ the owner of the small business concern identified below:

__X__ an official of the small business concern empowered to act on behalf of the concern identified below:

Name of Small Concern:
SUMMIT MICROELECTRONICS, INC.

Address of Small Concern:
300 ORCHARD CITY DRIVE, SUITE 131
CAMPBELL, CA 95008

I hereby declare that the above identified small business concern qualifies as a small business concern, as provided in 37 CFR 1.9(d), for purpose of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons.

I hereby declare that the rights under contract or law have been conveyed to, and remain with, the concern identified above with regard to the invention described in

__X__ the specification filed herewith, with title and inventor(s) as listed above.
____ the application identified above.
____ the patent identified above.

If the rights held by the above identified concern are not exclusive, each individual, concern, or organization having rights in the invention is listed below and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c), it that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization having any rights in the invention in addition to the above identified concern is listed below:
Name _____
Address _____
____ Individual __X__ Small Business ____ Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small business entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further, that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

RICHARD PALM
Print Name of Person Signing

VICE PRESIDENT MARKETING
Title of Person Signing

SUMMIT MICROELECTRONICS, INC., 300 Orchard City Drive, Suite 131, Campbell, CA 95008
Address of Person Signing

SIGNATURE _____ Date Jan 31, 2000

Application

For

United States Utility Patent

Title:

SELECTABLE ANALOG FUNCTIONS ON A CONFIGURABLE DEVICE AND METHOD EMPLOYING NONVOLATILE MEMORY

Inventors:

Theodore Martin Myers, residing at 647 Parma Way, Los Altos, CA 94024, a citizenship of the United States.

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SELECTABLE ANALOG FUNCTIONS ON A CONFIGURABLE DEVICE AND METHOD EMPLOYING NONVOLATILE MEMORY

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to the field of integrated circuit, and particularly to a configurable integrated circuit employing nonvolatile memory.

Description of Related Art

Power management integrated circuit market is growing rapidly for applications ranging from telecommunications, wireless devices, adaptive automotive systems, home appliances, to Internet security. Power management chips operate cooperatively with microprocessors for controlling various functions on a system. Consumer electronics, handheld devices, and desktop computers may require an integrated circuit to have different analog specifications and signal couplings with external chips.

Conventional power management chips provide outputs with digital values without analog output capabilities. For example, many analog functions require transistors to operate at a higher voltage than the typically 5 volts in a digital system. Other conventional power management chips provide separate integrated circuit device for each voltage level. More recently, manufacturers trim various internal reference voltages during wafer fabrication by burning fuses or via laser beams, which are limited to a one-time modification. None of these solutions are ideal due to their functional limitations and reduction in yield counts.

Accordingly, it is desirable to have a power management chip that provides an integrated circuit with configurable analog functions.

SUMMARY OF THE INVENTION

The invention discloses a configurable integrated circuit that enables a manufacturer or a customer to select the characteristics of analog functions and analog outputs for communication with external chips. The configurable integrated circuit employs nonvolatile (NV) memory with programmable bits including electrically erasable cells (E^2 cells), for customizing a specific circuit configuration. Activation or de-assertion of NV bits trims or selects analog functions including internal voltage thresholds, reset circuits, watchdog timers, voltage sensors, bandgap, and oscillating frequencies. NV bits also control a combination of analog circuits into digital outputs.

In an alternate embodiment, pin assignments on a configurable integrated circuit can be programmed through configuration registers. Pin assignments are directed to analog operations, such as programming pins to a no connect (electrically isolated), a watchdog timer reset input, and an active low drain output responding to a secondary voltage.

The use of NV registers provide the capability for programming multiple times in altering analog functions and settings. For example, a mother board can be assembled first in which a power management chip is programmed to with a set of analog functions and settings. The reverse is also applicable. A power management chip is first inserted on a mother board, where resistance and capacitance values can be adjusted or substituted to attain functional operation.

Optionally, the configurable integrated circuit contains actual analog circuits and functions that are selected by programming the nonvolatile memory, as opposed to a blank chip such as a blank ASIC. For example, the configurable integrated circuit is

designed to include four power management channels. If one of the four power management channels is not used, the unused power management channel is disabled, while the other three power management channels are enabled.

Advantageously, the present invention reduces costs by trimming internal voltages during a final manufacturing test or board level test of an integrated circuit chip. The present invention also advantageously provides a fast turnaround time by changing analog functions in a device configuration by programming nonvolatile memory. Furthermore, the present invention allows a customer to qualify one part for use with different and customized application.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a configurable microprocessor supervisory device with a nonvolatile memory in accordance with the present invention.

FIG. 2 is a flow chart illustrating the configurable microprocessor supervisory device with a nonvolatile memory in accordance with the present invention.

FIGS. 3A-3D are table diagrams illustrating bit assignments for bytes 0 through 3 in configuration registers in a configurable microprocessor supervisory device in accordance with the present invention.

FIG. 4 is a diagram illustrating an alternate embodiment in a configurable microprocessor supervisory device for programming pin assignments in accordance with the present invention.

FIG. 5 is a block diagram in combining analog outputs to generate a digital output in accordance with the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

FIG. 1 is an architectural diagram of a configurable microprocessor supervisory device **10** which employs a nonvolatile (NV) memory **11**. Configurable microprocessor supervisory device **10** includes NV memory **11** having configuration registers **12-15**, an x-to-y decoder **16**, a first configuration **17**, a second configuration **18**, a third configuration **19**, and an n configuration **20**. Configurable microprocessor supervisory device **10** provides a range of analog functions and output levels which are selectable by programming the bits in NV register **12**, **13**, **14**, and **15**. Decoder **16** decodes through a line **21** of programmable bits in configuration register **12**, a line **22** of programmable bits in configuration register **13**, a line **23** of programmable bits in configuration register **14**, or a line **24** of programmable bits in configuration register **15**. The result of decoding configuration registers **12-15** produces a device configuration as either first configuration **17** via a line **25**, second configuration **18** via a line **26**, third configuration **19** via a line **27**, and n configuration **20** via a line **28**.

A manufacturer or user initially determines a desirable set of analog functions in configurable microprocessor supervisory device **10**. Configurable microprocessor supervisory device **10** then becomes one of the configurations as first configuration **16**, second configuration **17**, third configuration **18**, or n configuration **19**. The configuration in microprocessor supervisory device **10** is determined by the programmable bits in NV registers **13**, **14**, and **15**. Each bit or a combination of bits in NV registers **13**, **14**, and **15** corresponds to activating or deactivating an analog function, or increasing or decreasing an activated analog function. Optionally, one skilled in the art should recognize that

digital functions, or a combination of digital and analog functions can be integrated on configurable microprocessor supervisory device **10** for selection by NV registers **12-15**.

FIG. 2 is a flow chart of configurable microprocessor supervisory method **20** with non-volatile memory **11**. A manufacturer or user selects **31** a certain combinations of analog functions and output levels for operation with a microprocessor (not shown). The combination of analog functions and output levels corresponds with first configuration **17**, second configuration **18**, third configuration **19**, or n configuration **20**. A manufacturer or user programs **32** certain nonvolatile bits in configuration registers **12**, **13**, **14**, and **15** which correspond and enable the selected combinations of analog functions and output levels. An analog function or output level may have a range of settings. Optionally, when an analog function is enabled in step **32**, the manufacturer or user programs **33** nonvolatile bits in configuration registers **12**, **13**, **14**, and **15** to set a specific analog value associated with that enabled analog function. As a result of selecting the desirable combination of analog functions by programming configuration registers **12-15**, first configuration **17**, second configuration **18**, third configuration **19**, or n configuration **20** is generated on configurable microprocessor supervisory device **10**.

FIGS. 3A-3D are table diagrams that illustrates one embodiment of configurable microprocessor supervisory device **10** with four configuration registers. Each NV registers corresponds to a specified byte, namely, configuration register **12** storing byte 0, configuration register **13** storing byte 1, configuration register **14** storing byte 2, and configuration register **15** storing byte 3.

FIG. 3A is a table diagram showing bit assignments of byte 0 of configuration register **12**. The reset voltage range on configurable microprocessor supervisory device

10 is selected by programming bits 4-0 in byte 0. Depending on the binary value of $byte_0$[4:0] in configuration register **12**, a corresponding reset voltage is selected. More specifically, the reset voltage is set as follows: if $byte_0$[4:0] is programmed with a binary value of "10000", "01000", "00100", "00010", and "00001", the reset voltage is set respectively to 4.625, 4.375, 2.9, 2.65, and 2.15 volts. The duration of a reset timeout on configurable microprocessor supervisory device **10** is programmable through the selection in bits 5 and 6 in byte 0. The reset timeout is set at 200ms when $byte_0$[6:5] = "11", set at 100ms when $byte_0$[6:5] = 10, set at 50ms when $byte_0$[6:5] = "01", and set at 25ms when $byte_0$[6:5] = "00".

FIG. 3B is a table diagram showing the bit assignments of byte 1 of configuration register **13**. Byte 1 contains NV bits for selecting write enable, V_{sense} voltage, responding to all addresses, device identifier code, and watchdog interval. The duration of a watchdog interval is programmable through bits 2-0 in byte 1. When $byte_1$[2:0] is programmed as "111", "110", "101", "100", "011" in binary value, the corresponding watchdog interval is equal to 6.4 seconds, 3.2 seconds, 1.6 seconds, 0.8 second, and 0.4 seconds respectively. The watchdog timer is in an OFF state when $byte_1$[2:0] = 00X. A device identifier code is selected by programming bit 3 in byte 1 such that the device is responds to "1011" if $byte_1$[3] is programmed with a "1" and responds to "1010" if $byte_1$[3] is programmed with a "0".

Bit 4 of byte 1 in configuration register **13** designates whether configurable microprocessor supervisory device **10** responds to all addresses or responds to pin addresses. Configurable microprocessor supervisory device **10** responds to all addresses if $byte_2$[4] = "1" and responds to all pin addresses if $byte_2$[4] = "0". Table 1 below further

shows the designation of bit 4 for each of the eight parts in this embodiment. Bit 5 of byte 1 of configuration register **13** indicates whether V_{sense} is undervoltage or overvoltage. V_{sense} is undervoltage when $byte_2[5]$ = "1" while V_{sense} is overvoltage when $byte_2[5]$ = "1". Bit 6 of byte 1 turns ON or OFF A complete configuration write enable signal. The write enable signal is disabled if $byte_2[6]$ = "1" and is enabled if $byte_2[6]$ = "0".

Table 1

Part No.	Byte 1: bit 4	Other Functions
Part 1	Set low to respond to pin addresses.	Pin 7 has an internal pulldown on this pin. This pin may float or tie low.
Part 2	Set high to respond to all addresses. If byte 1:bit 4 is set low, then the part responds to A1 on pin1 and A2 on pin 3. A0 is a don't care.	
Part 3	Set high to respond to all addresses. If byte 1:bit 4 is set low, then the part will respond to A1 on pin1 and A2 on pin3. A0 is a don't care.	
Part 4	Set high to respond to all addresses. If byte1:bit4 is set low, then this part responds to A2 on pin3. A0 and A1 are don't care.	
Part 5	Set high to respond to all addresses.	Both resets respond to Vcc low, RESETN_in, and V_{SENSE}
Part 6	Respond to all addresses regardless of the setting of byte1:bit 4.	
Part 7	Respond to all addresses regardless of the setting of byte1:bit 4.	
Part 8	Set low to respond to pin addresses.	

FIG. 3C is a table diagram showing the bit assignments of byte 2 of configuration register **14**. Byte 2 includes programmable bits for trimming the V_{sense} voltage or

bandgap, for trimming the frequency of an oscillator, or for selecting whether to utilize full or half memory capacity. The V_{sense} voltage is trimmed by programming bits 3-0 of byte 2 of configuration register **14** where the V_{sense} voltage is trimmed to a lower value if $byte_3[3:0]$ = "1111" while the V_{sense} voltage is increased to a higher value if $byte_3[3:0]$ = "0000". The trimming of the V_{sense} voltage can be an iterative process in which the voltage trimming is repeated until the desirable V_{sense} voltage is attained. The allocation of full or half memory is programmable through bit 4 of byte 2. Full memory is utilized when $byte_3[4]$ = "1" and only half memory is utilized when $byte_3[4]$ = "0". In this illustration, although 4K or 16K represents a full memory while 2K or 8K represents half memory, one skilled in the art should recognize that the value of full or half memory capacity can be adjusted depending a designer's choice. The oscillator's frequency is trimmed by programming bits 7-5 in byte 2 in configuration register **14**. The frequency of the oscillator is reduced if $byte_3[7-5]$ = "111". To increase the frequency of the oscillator, the value of $byte_3[7-5]$ is set to "000". Similarly, this process can be repeated to further decrease or increase the frequency setting of the oscillator until a desirable frequency is obtained.

FIG. 3D is a table diagram showing bit assignments of byte 3 of configuration register **15**. Byte 3 includes programming bits for trimming a V_{trip} voltage, for selecting a full or half memory, and for enabling a configuration write disable signal. The V_{trip} voltage is trimmed by setting $byte_4[3:0]$ = "1111". To increase the V_{trip} voltage, $byte_4[3:0]$ are set to "0000". This process can be repeated to further decrease or increase the V_{trip} voltage until the desirable V_{trip} voltage is reached. Bits 6-4 in byte 3 of configuration register **15** select full or half memory for a particular configuration. When

$byte_4[6:4]$ = "111", the full/half memory for a part 8 or an eighth configuration is selected. . When $byte_4[6:4]$ = "110", the full/half memory for a part 7 or a seventh configuration is selected. When $byte_4[6:4]$ = "101", "100", "011", "010", "001", and "000", the full/half memory is respectively selected for a part 6 or a sixth configuration, a part 5 or a fifth configuration, a part 4 or a fourth configuration, a part 3 or third configuration **19**, a part 2 or second configuration **18**, and part 1 or first configuration **17**. The configuration write disable signal is programmed through bit 7 in byte 3 of configuration register **15** where the configuration write enable is enabled if $byte_4[7]$ = "0" and the configuration write enable is disabled when $byte_4[7]$ = "1". Additional registers divided as trim registers and as configuration registers are illustrated in hexadecimal numbers in Appendixes A and B.

In an alternate embodiment, configuration registers in NV memory **11** are used to designate pin assignments. Configurable microprocessor supervisory device **10** is a configurable integrated circuit with eight pins which can be programmed to operate as one of the eight parts. The pin assignments for device **10** is configured as follows: if programmed as part 1, then pins 1 through 8 are assigned with pin 1 as NC, pin 2 as RESET#, pin 3 as NC, pin 4 as Gnd, pin 5 as SDA, pin 6 as SCL, pin 7 as RESET, and pin 8 as VCC; if programmed as part 2, then pins 1 through 8 are assigned with pin 1 as NC, pin 2 as RESET#, pin 3 as NC, pin 4 as Gnd, pin 5 as SDA, pin 6 as SCL, pin 7 as NC, and pin 8 as VCC; if programmed as part 3, then pins 1 through 8 are assigned with pin 1 as A0, pin 2 as A1, pin 3 as A2, pin 4 as Gnd, pin 5 as SDA, pin 6 as SCL, pin 7 as NC, and pin 8 as VCC; if programmed as part 4, then pins 1 through 8 are assigned with pin 1 as WDI, pin 2 as RESET#, pin 3 as NC, pin 4 as Gnd, pin 5 as SDA, pin 6 as SCL,

pin 7 as RESET, and pin 8 as VCC; if programmed as part 5, then pins 1 through 8 are assigned with pin 1 as VLOW, pin 2 as RESET#, pin 3 as VSENSE, pin 4 as Gnd, pin 5 as SDA, pin 6 as SCL, pin 7 as RESET, and pin 8 as VCC; if programmed as part 6, then pins 1 through 8 are assigned with pin 1 as RESET#2, pin 2 as RESET#, pin 3 as VSENSE, pin 4 as Gnd, pin 5 as SDA, pin 6 as SCL, pin 7 as MR#, and pin 8 as VCC; if programmed as part 7, then pins 1 through 8 are assigned with VLOW#, pin 2 as RESET, pin 3 as VSENSE, pin 4 as Gnd, pin 5 as SDA, pin 6 as SCL, pin 7 as WDI, and pin 8 as VCC; if programmed as part 8, then pins 1 through 8 are assigned with pin 1 as A0, pin 2 as A1, pin 3 as A3, pin 4 as Gnd, pin 5 as SDA, pin 6 as SCL, pin 7 as RESET#, and pin 8 as VCC. Table 2 below further shows the pin assignments as described in FIG. 4.

Table 2

Pin#	Part 8	Part 7	Part 6	Part 5	Part 4	Part 3	Part 2	Part 1
1	A0	A1	A1	WDIB	RESETB1	VLOWB	VLOWB	A0
2	A1	RESETB	RESETB	RESETB	RESETB2	RESETB	RESETB	A1
3	A2	A2	A2	A2	VSENSE	VSENSE	VSENSE	A2
4	GND	GND	GND	GND	GND	GND	GND	GND
5	SDA	SDA	SDA	SDA	SDA	SDA	SDA	SDA
6	SCL	SCL	SCL	SCL	SCL	SCL	SCL	SCL
7	NC	NC/RESET	WP	RESET	RESETB_ in	WDI	WDI	RESETB
8	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC

Various control settings and modifications of configuration registers **12-15** are within the spirit of the present invention. For example, configuration registers **12-15** can be set at the factory and then locked so that a user just receives a standard part and is not

aware that the part is programmable. Or, two configuration registers **12** and **13** can be accessed by a user with the other two configuration registers **14** and **15** are locked. Or, all four configuration registers **12-15** can be accessed by the user and then locked if the user choose to trim analog functions and to select a device interface among multiple possible interfaces.

FIG. 5 is a block diagram **40** in combining multiple analog outputs in generating a digital output. The block diagram **40** is integrated in configurable microprocessor supervisory device **10** and includes an analog subcircuit **41**, an analog subcircuit **42**, an analog subcircuit **43**, and a logic gate **44**. Logic gate **44**, such as an OR gate or an AND gate, receives an analog output **45**, an analog output **46**, and an analog output **47** for generate a digital output **48**. An example of digital output **48** is an interrupt request signal, IRQ#, which collects from various analog signals to produce the IRQ# signal.

The above embodiments are only illustrative of the principles of this invention and are not intended to limit the invention to the particular embodiments described. For example, it is apparent to one skilled in the art that nonvolatile memory **11** can include as many configuration registers as needed to program various combinations of analog functions, digital functions, pin assignments, internal voltages, and external voltages. Moreover, one skilled in the art should recognize that a device configuration can be made dynamic such that an integrated circuit device can be re-configured during each power up or by the reception of an external control signal. Accordingly, various modifications, adaptations, and combinations of various features of the described embodiments can be practiced without departing from the scope of the invention as set forth in the appended claims.

APPENDIX A

Trim Register	Bit Assignments	Description
0	7-4	Not used
	3	Configuration Write Disable XXXX 1XXX Write Disable XXXX 0XXX Write Enable
	2-0	Oscillator Trim XXXX X111 Slower XXXX X000 Faster
1	7-5	Not Used
	4-0	Slew Rate Trim XXX1 1111 Faster XXX0 0000 Slower
2	7-4	Temp Comp TIR Current Trim 1111 XXXX Higher 0000 XXXX Lower
	3-0	Flat Across Temp Current Trim XXXX 1111 Higher XXXX 0000 Lower
3	7-4	Temp Comp Amp Gain Trim 1111 XXXX Higher 0000 XXXX Lower
	3-0	Bandgap Trim XXXX 1111 Lower XXXX 0000 Higher
4	7-0	Temp Sense Amp Trim 1111 1111 Higher 0000 0000 Lower
5	7-6	CB_D Trip Adjustment 11XX XXXX Higher 00XX XXXX Lower
	5-4	CB_C Trip Adjustment

		XX11 XXXX Higher XX00 XXXX Lower
	3-2	CB_B Trip Adjustment XXXX 11XX Higher XXXX 00XX Lower
	1-0	CB_A Trip Adjustment XXXX XX11 Higher XXXX XX00 Lower
6	7-5	Not Used
	4-0	Tamp Offset Trim XX11 1111 Higher XX00 0000 Lower
7	7-0	Overvoltage/Undervoltage2 Current Trim 1111 1111 Higher 0000 0000 Lower

APPENDIX B

Configuration Register	Bit Assignments	Description
0	7-0	Bus side A undervoltage trip point 1111 1111 higher 0000 0000 lower
1	7-0	Bus side B undervoltage trip point 1111 1111 higher 0000 0000 lower
2	7-0	Bus side C undervoltage trip point 1111 1111 higher 0000 0000 lower
3	7-0	Bus side D undervoltage trip point 1111 1111 higher 0000 0000 lower
4	7	Bus side A undervoltage enable 1XXXX XXXX enable 0XXXX XXXX disable
	6	Bus side A overvoltage enable X1XX XXXX enable X0XX XXXX disable
	5-0	Bus side A overvoltage offset XX11 1111 higher XX00 0000 lower
5	7	Bus side B undervoltage enable 1XXXX XXXX enable 0XXXX XXXX disable
	6	Bus side B overvoltage enable X1XX XXXX enable X0XX XXXX disable
	5-0	Bus side B overvoltage offset XX11 1111 higher XX00 0000 lower

6		Bus side C undervoltage enable
	7	1XXXX XXXX enable
		0XXXX XXXX disable
	6	Bus side B overvoltage enable
		X1XX XXXX enable
		X0XX XXXX disable
	5-0	Bus side B overvoltage offset
		XX11 1111 higher
		XX00 0000 lower
7		Bus side D undervoltage enable
	7	1XXXX XXXX enable
		0XXXX XXXX disable
	6	Bus side B overvoltage enable
		X1XX XXXX enable
		X0XX XXXX disable
	5-0	Bus side B overvoltage offset
		XX11 1111 higher
		XX00 0000 lower
8	7 - 0	Card side A undervoltage trip point
		1111 1111 higher
		0000 0000 lower
9	7 - 0	Card side B undervoltage trip point
		1111 1111 higher
		0000 0000 lower
A	7 - 0	Card side C undervoltage trip point
		1111 1111 higher
		0000 0000 lower
B	7 - 0	Card side D undervoltage trip point
		1111 1111 higher
		0000 0000 lower
C	7	Not used
	6	Soft start enable supply A
		X1XX XXXX enable
	5-0	X0XX XXXX disable

		Card side A overvoltage offset XX11 1111 higher XX00 0000 lower
D	7	Not used
	6	Soft start enable supply B X1XX XXXX enable X0XX XXXX disable
	5-0	Card side A overvoltage offset XX11 1111 higher XX00 0000 lower
E	7	Not used
	6	Soft start enable supply C X1XX XXXX enable X0XX XXXX disable
	5-0	Card side A overvoltage offset XX11 1111 higher XX00 0000 lower
F	7	Not used
	6	Soft start enable supply D X1XX XXXX enable X0XX XXXX disable
	5-0	Card side A overvoltage offset XX11 1111 higher XX00 0000 lower
10	7	Responds to all addresses 1XXX XXXX respond to all addresses 0XXX XXXX respond to pin addresses
	6	Change device identifier code X1XX XXXX respond to 1011 X0XX XXXX respond to 1010
	5-4	Tracker over/under 300mv action XX11 XXXX generate IRQ XX10 XXXX shut down all XX01 XXXX shut down bad channel XX00 XXXX do nothing

	3-2	Tracker slew rate rising XXXX 11XX 1000 v/s XXXX 10XX 500 v/s XXXX 01XX 250 v/s XXXX 00XX 100 v/s
	1-0	Tracker slew rate falling XXXX 11XX 1000 v/s XXXX 10XX 500 v/s XXXX 01XX 250 v/s XXXX 00XX 100 v/s
11	7	Bus side A undervoltage 1XXX XXXX triggers reset 0XXX XXXX does not trigger reset
	6	Bus side B undervoltage X1XX XXXX triggers reset X0XX XXXX does not trigger reset
	5	Bus side C undervoltage XX1X XXXX triggers reset XX0X XXXX does not trigger reset
	4	Bus side D undervoltage XXX1 XXXX triggers reset XXX0 XXXX does not trigger reset
	3	Bus side A overvoltage XXXX 1XXX triggers reset XXXX 0XXX does not trigger reset
	2	Bus side B overvoltage XXXX X1XX triggers reset XXXX X0XX does not trigger reset
	1	Bus side C overvoltage XXXX XX1X triggers reset XXXX XX0X does not trigger reset
	0	Bus side D overvoltage XXXX XXX1 triggers reset XXXX XXX0 does not trigger reset

12	7	Card side A undervoltage 1XXX XXXX triggers reset 0XXX XXXX does not trigger reset
	6	Card side B undervoltage X1XX XXXX triggers reset X0XX XXXX does not trigger reset
	5	Card side C undervoltage XX1X XXXX triggers reset XX0XX XXXX does not trigger reset
	4	Card side D undervoltage XXX1 XXXX triggers reset XXX0 XXXX does not trigger reset
	3	Card side A undervoltage#2 XXXX 1XXX triggers reset XXXX 0XXX does not trigger reset
	2	Card side B undervoltage#2 XXXX X1XX triggers reset XXXX X0XX does not trigger reset
	1	Card side C undervoltage#2 XXXX XX1X triggers reset XXXX XX0X does not trigger reset
	0	Card side D undervoltage#2 XXXX XXX1 triggers reset XXXX XXX0 does not trigger reset
13	7	Bus side A undervoltage 1XXX XXXX triggers IRQ# 0XXX XXXX does not trigger IRQ#
	6	Bus side B undervoltage X1XX XXXX triggers IRQ# X0XX XXXX does not trigger IRQ#
	5	Bus side C undervoltage XX1X XXXX triggers IRQ# XX0X XXXX does not trigger IRQ#
	4	Bus side D undervoltage

		XXX1 XXXX triggers IRQ# XXX0 XXXX does not trigger IRQ#
	3	Bus side A overvoltage XXXX 1XXX triggers IRQ# XXXX 0XXX does not trigger IRQ#
	2	Bus side B overvoltage XXXX X1XX triggers IRQ# XXXX X0XX does not trigger IRQ#
	1	Bus side C overvoltage XXXX XX1X triggers IRQ# XXXX XX0X does not trigger IRQ#
	0	Bus side D overvoltage XXXX XXX1 triggers IRQ# XXXX XXX0 does not trigger IRQ#
14	7	Card side A undervoltage 1XXX XXXX triggers IRQ# 0XXX XXXX does not trigger IRQ#
	6	Card side B undervoltage X1XX XXXX triggers IRQ# X0XX XXXX does not trigger IRQ#
	5	Card side C undervoltage XX1X XXXX triggers IRQ# XX0X XXXX does not trigger IRQ#
	4	Card side D undervoltage XXX1 XXXX triggers IRQ# XXX0 XXXX does not trigger IRQ#
	3	Card side A undervoltage#2 XXXX 1XXX triggers IRQ# XXXX 0XXX does not trigger IRQ#
	2	Card side B undervoltage#2 XXXX X1XX triggers IRQ# XXXX X0XX does not trigger IRQ#
	1	Card side C undervoltage#2 XXXX XX1X triggers IRQ#

		XXXX XX0X does not trigger IRQ#
	0	Card side D undervoltage#2 XXXX XXX1 triggers IRQ# XXXX XXX0 does not trigger IRQ#
15	7	Bus side A undervoltage IRQ# fault (volatile) 1XXX XXXX fault 0XXX XXXX no fault
	6	Bus side B undervoltage IRQ# fault (volatile) X1XX XXXX fault X0XX XXXX no fault
	5	Bus side C undervoltage IRQ# fault (volatile) XX1X XXXX fault XX0X XXXX no fault
	4	Bus side D undervoltage IRQ# fault (volatile) XXX1 XXXX fault XXX0 XXXX no fault
	3	Bus side A overvoltage IRQ# fault (volatile) XXXX 1XXX fault XXXX 0XXX no fault
	2	Bus side B overvoltage IRQ# fault (volatile) XXXX X1XX fault XXXX X0XX no fault
	1	Bus side C overvoltage IRQ# fault (volatile) XXXX XX1X fault XXXX XX0X no fault
	0	Bus side D overvoltage IRQ# fault (volatile) XXXX XXX1 fault XXXX XXX0 no fault
16	7	Card side A undervoltage IRQ# fault (volatile) 1XXX XXXX fault 0XXX XXXX no fault
	6	Card side B undervoltage IRQ# fault (volatile) X1XX XXXX fault X0XX XXXX no fault

	5	Card side C undervoltage IRQ# fault (volatile) XX1X XXXX fault XX0X XXXX no fault
	4	Card side D undervoltage IRQ# fault (volatile) XXX1 XXXX fault XXX0 XXXX no fault
	3	Card side A overvoltage IRQ# fault (volatile) XXXX 1XXX fault XXXX 0XXX no fault
	2	Card side B overvoltage IRQ# fault (volatile) XXXX X1XX fault XXXX X0XX no fault
	1	Card side C overvoltage IRQ# fault (volatile) XXXX XX1X fault XXXX XX0X no fault
	0	Card side D overvoltage IRQ# fault (volatile) XXXX XXX1 fault XXXX XXX0 no fault
17	7-6	Unused
	5-3	Long dog XX11 1XXX 6.4ms XX11 0XXX 3.2ms XX10 1XXX 1.6ms XX10 0XXX 0.8ms XX0X XXXX off
	2-0	XXXX X111 3.2s XXXX X110 1.6s XXXX X101 0.8s XXXX X100 0.4s XXXX X0XX off

We Claim:

1. A method for programming a configurable integrated circuit, comprising the steps of:

programming a plurality of nonvolatile bits in one or more nonvolatile registers, each nonvolatile bit or a combination of nonvolatile bits in the plurality of nonvolatile bits corresponding to an analog function; and

generating a configuration on an integrated circuit from programming the plurality of nonvolatile bits in the one or more nonvolatile registers.

2. The method of Claim 1 wherein the plurality of nonvolatile bits in the one or more nonvolatile registers comprises E^2 cells.

3. The method of Claim 1 wherein in the programming step comprises the step of enabling an analog function by the nonvolatile bit or the combination of nonvolatile bits.

4. The method of Claim 3 wherein in the enabling step comprises the step of setting the analog function to a specific value.

5. The method of Claim 1 wherein in the programming step comprises changing pin assignments by programming one or more nonvolatile bits.

6. The method of Claim 1 wherein the analog function comprises trimming an internal voltage of the integrated circuit.

7. The method of Claim 1 further comprising the step of combining a plurality of analog signals to generate a digital output.

8. The method of Claim 1 further comprising the step of storing a status of a fault condition of the integrated circuit in the one or more NV registers.

9. An integrated circuit, comprising:

one or more nonvolatile registers having a plurality of nonvolatile bits, each nonvolatile bit or a combination of nonvolatile bits in the plurality of nonvolatile bits corresponding to programming an analog function; and

a circuit configuration in the integrated circuit being generated from programming one or more nonvolatile registers.

10. The integrated circuit of Claim 9 further comprising a decoder, coupled between the one or more nonvolatile registers and a circuit configuration, for decoding the plurality of nonvolatile bits for programming analog functions.

11. The integrated circuit of Claim 9 wherein the plurality of nonvolatile bits comprises E^2 cells.

12. The integrated circuit of Claim 9 wherein the nonvolatile bit or the combination of nonvolatile bits in the one or more nonvolatile registers enables the analog function.

13. The integrated circuit of Claim 12 wherein the nonvolatile bit or the combination of nonvolatile bits in the one or more nonvolatile registers sets a specific value to the enabled analog function.

14. The integrated circuit of Claim 9 wherein the nonvolatile bit or the combination of nonvolatile bits in the one or more nonvolatile registers changes pin assignments of the integrated circuit.

15. The integrated circuit of Claim 12 where the bit or the combination of nonvolatile bits trims an internal voltage of the enabled analog function.

16. The integrated circuit of Claim 9 further comprising a logic gate for combining a plurality of analog signals to generate a digital output.

17. A configurable device, comprising:

means for programming one or more nonvolatile registers having a plurality of nonvolatile bits, each bit or a combination of bits in the plurality of nonvolatile bits corresponding to an analog function; and

means for generating a configuration from programming the plurality of nonvolatile bits.

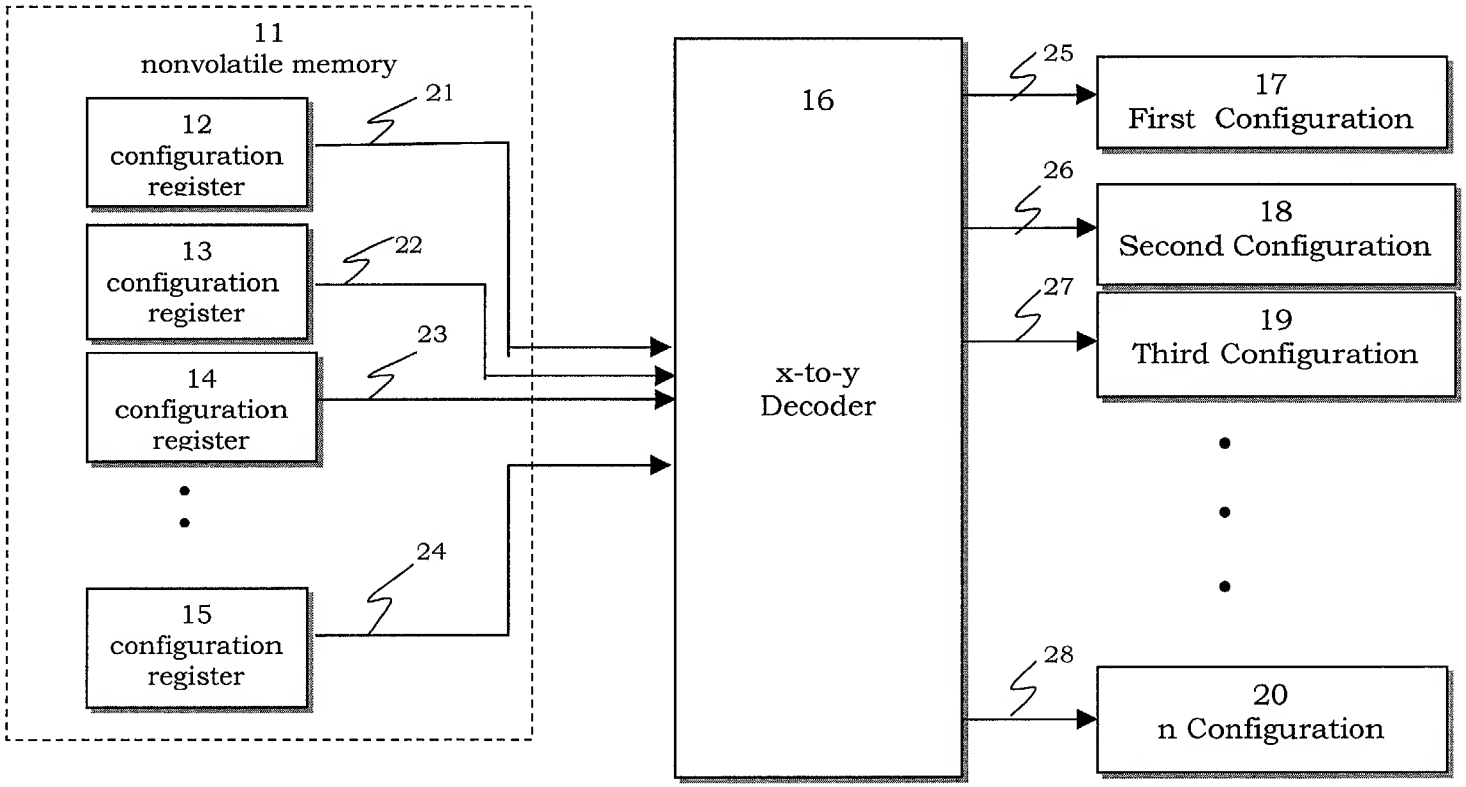
18. The configurable device of Claim 17 wherein the programming means of the one or more nonvolatile registers comprises E^2 cells.

19. The configurable device of Claim 17 wherein the programming means comprises enabling the analog function.

20. The configurable device of Claim 17 wherein the programming means comprises selecting a specific value of the analog function.

ABSTRACT

A configurable integrated circuit and method for trimming a desirable combination of analog and digital functions and customizing pin assignments by programming nonvolatile memory. Functional enhancement and chip compatibility are achieved by configuring an integrated circuit with specified analog and digital settings for operation with an external chip. Multiple NV registers with designated bits that correspond to activating, deactivating, trimming, or changing analog functions including internal voltages, bandgap, and oscillating frequencies.



10

FIGURE 1

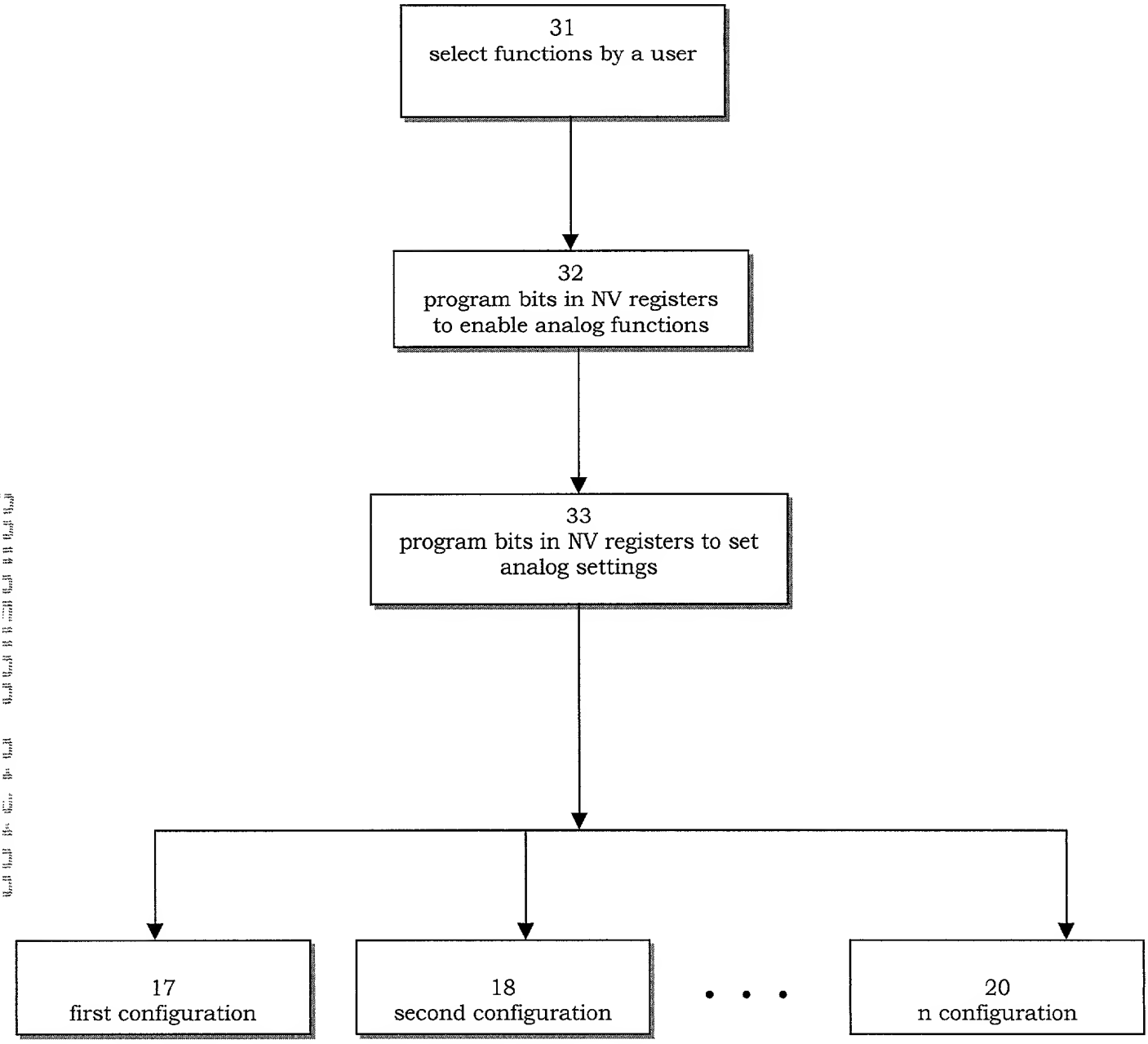

31
select functions by a user
32
program bits in NV registers
to enable analog functions
33
program bits in NV registers to set
analog settings
17
first configuration
18
second configuration
20
n configuration
30

FIGURE 2

Byte 0

Bits 6-5	Reset timeout	Bits 4-0	Reset range
11	200ms	10000	4.625
10	100ms	01000	4.375
01	50ms	00100	2.9
00	25ms	00010	2.65
		00001	2.15

FIGURE 3A

Byte 1

Bit 6	Complete config write disable	Bit 5	Vsense overvoltage/undervoltage	Bit 4	Responds to all addresses
1	Write disable	1	Undervoltage	1	Respond to all addresses
0	Write enable	0	Overvoltage	0	Respond to pin addresses

Bit 3	Change device identifier code	Bits 2-0	Watchdog interval
1	Respond to 1011	111	6.4s
0	Respond to 1010	110	3.2s
		101	1.6s
		100	.8s
		011	.4s
		00X	off

FIGURE 3B

Byte 2

Bits 7-5	Osc Trim	Bit 4	Full Mem/ Half Mem	Bits 3-0	Bandgap (Vsense) trim
111	Slower	1	4K/16K	1111	Lower
000	Faster	0	2K/8K	0000	Higher

FIGURE 3C

Byte 3

Bit 7	Config write disable	Bits 6-4	Full Mem/ Half Mem	Bits 3-0	Vtrip trim
1	Write disable	111	Part 8	1111	Lower
0	Write enable	110	Part 7	0000	Higher
		101	Part 6		
		100	Part5		
		011	Part4		
		010	Part3		
		001	Part2		
		000	Part1		

FIGURE 3D

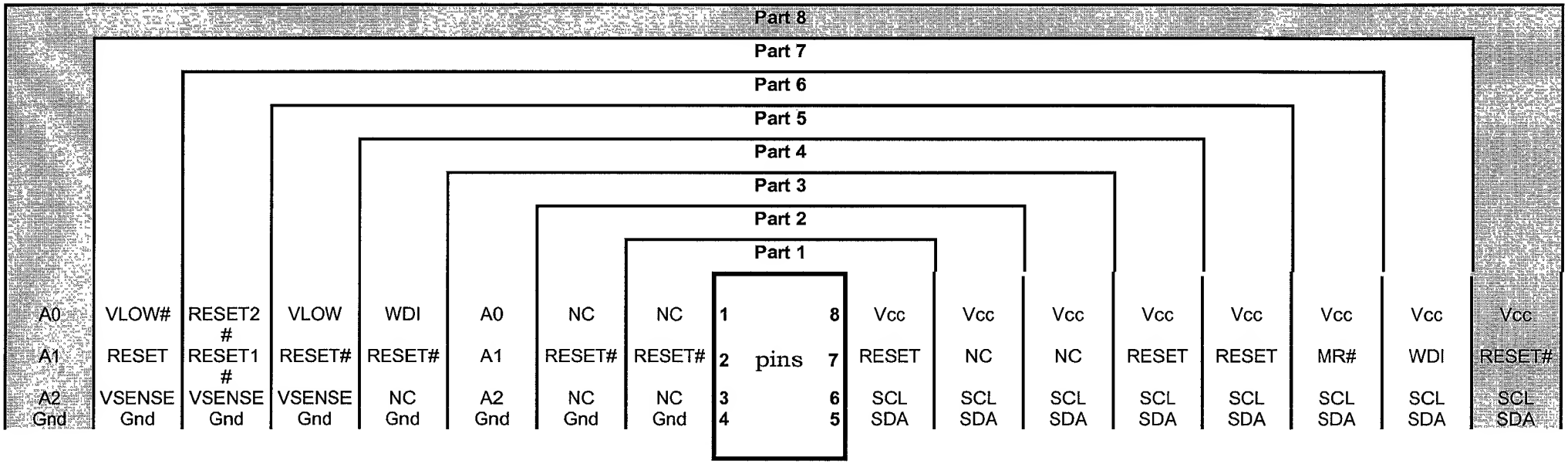
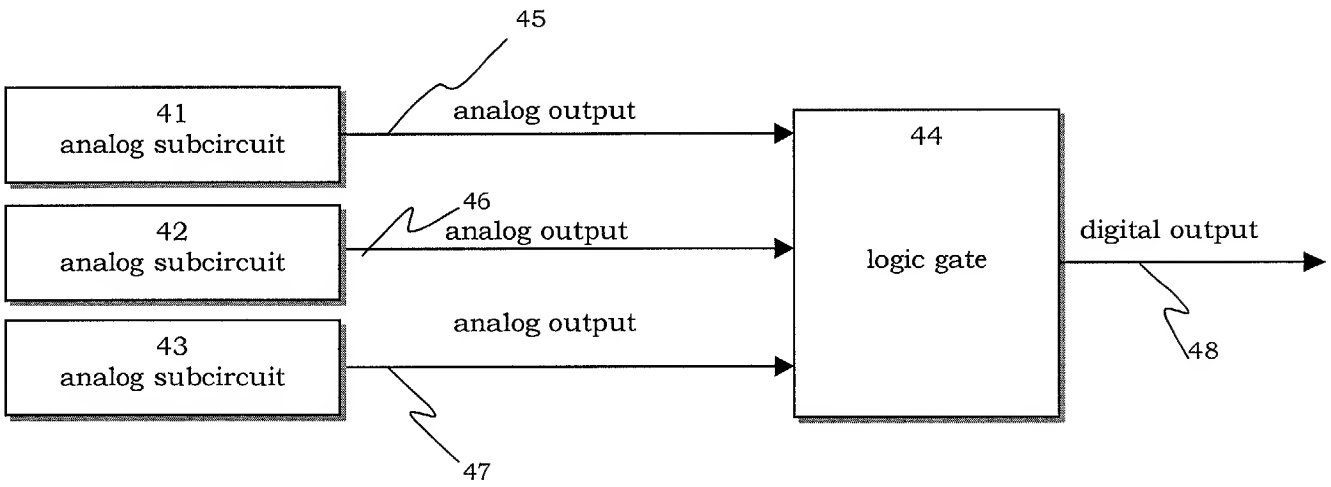

Part 8
Part 7
Part 6
Part 5
Part 4
Part 3
Part 2
Part 1
A0 VLOW# RESET2# VLOW WDI A0 NC NC 1 8 Vcc Vcc Vcc Vcc Vcc Vcc Vcc Vcc
A1 RESET RESET1# RESET# RESET# A1 RESET# RESET# 2 pins 7 RESET NC NC RESET RESET MR# WDI RESET#
A2 VSENSE VSENSE VSENSE NC A2 NC NC 3 6 SCL SCL SCL SCL SCL SCL SCL SCL
Gnd Gnd Gnd Gnd Gnd Gnd Gnd Gnd 4 5 SDA SDA SDA SDA SDA SDA SDA SDA

FIGURE 4


45
41
analog subcircuit
analog output
44
46
42
analog subcircuit
analog output
logic gate
digital output
analog output
43
analog subcircuit
48
47

40

FIGURE 5

Docket No: **SUMT-P001**

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, postal address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original first and joint inventor (if multiple names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SELECTABLE ANALOG FUNCTIONS ON A CONFIGURABLE DEVICE AND METHOD EMPLOYING NONVOLATILE MEMORY

the specification of which is attached hereto unless the following information is indicated:

_____ was filed on _____;
as United States Application Number or PCT International Application Number _____;
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendments referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified, as so indicated below, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

_____ (Application No.)	_____ (Day/Month/Year Filed)

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. 1.56 that became available between the filing date of the prior application and the national or PCT International filing date of this application.

_____ (Application No.)	_____ (Day/Month/Year Filed)	_____ (Status - patented, pending, abandoned)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and beliefs are believed to be true; and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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